A NEW ERASE TECHNIQUE TO IMPROVE THE SOURCE LEAKAGE OF FLASH EPROM CELLS DURING SOURCE ERASE

ABSTRACT OF THE DISCLOSURE

In one aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a voltage pulse at the source of the semiconductor device and a multiple step voltage pulse of the opposite polarity at the gate of the semiconductor device. The multiple step voltage pulse comprises at least a first voltage pulse and a second voltage pulse at the gate of the semiconductor device. The second voltage pulse is usually greater in magnitude than the first voltage pulse.

In another aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a substantially constant positive voltage pulse for a first time interval, t_1, at the source of the semiconductor device. A first and then a second negative voltage pulse are also applied at the gate of the semiconductor device for a second and third time interval, t_2 and t_3, respectively. The second negative voltage pulse is greater in magnitude than the first negative voltage pulse. The negative and positive voltage pulses are substantially coincidental in time.